Experiment 4

Comparators, positive feedback, and relaxation oscillators

This experiment will continue our investigations of nonlinear analog circuits. We consider first a simple op-amp application used to *interface* an analog signal to a digital device: the *Schmitt trigger*, a 1-bit *analog to digital converter* (in which the op-amp is used as a *comparator*). This circuit introduces us to the use of *positive feedback* in our op-amp designs, rather than the negative feedback we've used so far. In this case the positive feedback is used both to introduce *hysteresis* in the circuit's *state transition* trigger conditions and to speed up the op-amp's output state transitions.

Next we couple a Schmitt trigger with first an *RC* low-pass filter and then an op-amp integrator circuit to develop *relaxation oscillators*, simple signal generators which work much like a ticking clock to output a repetitive waveform. Spend some time studying this relaxation oscillator idea, because its feedback scheme is applicable to many types of simple analog signal generators, clocks, and timers (some of which could more correctly be considered to be simple digital circuits).

We then introduce a special-purpose integrated circuit, the "555 timer," a versatile device we will use to build *astable* and *monostable multivibrator* circuits useful for a variety of applications. This device is our first true example of a *mixed-signal circuit* incorporating both analog and digital design concepts. Extending this digital design theme, we will conclude the text with a potpourri of comparator-based implementations of basic binary logic gate functions. Too slow for modern digital circuit applications, they are still quite useful if your design is mostly analog but needs a simple implementation of a couple of logic operations.

Because the fundamental behaviors of these circuits are very nonlinear, linear superposition will have to be applied most carefully (essentially limited to voltage dividers), and we must analyze the circuits' actions almost exclusively in the time domain.

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TABLE OF CIRCUITS

THE SCHMITT TRIGGER AND POSITIVE FEEDBACK

The op-amp as a "comparator"

Consider an op-amp used to amplify an input signal *without feedback* as shown in Figure 4-1. Because no feedback is used, the input signal is amplified by the op-amp's full open-loop gain, so even a tiny input voltage (on the order of a millivolt or less) will be enough to send the op-amp's output into saturation, as shown in the plots of v_{in} and v_{out}. Thus, in this case (since the op-amp's *+Input* is grounded), the output gives $-1 \times$ the sign of v_{in}, and the circuit is in essence a one-bit *analog to digital converter* (*ADC*), also called a *comparator*.

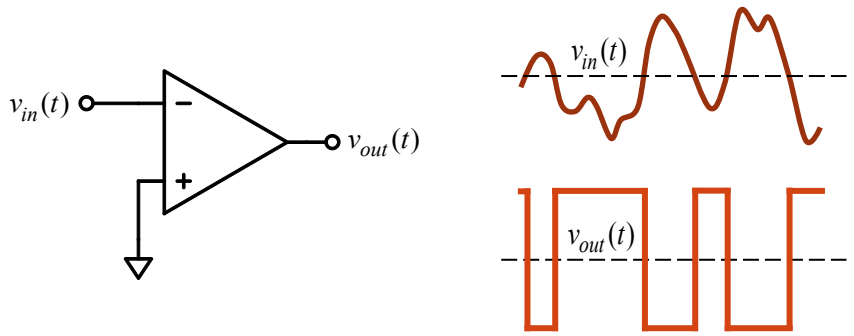


Figure 4-1: An op-amp used as a *comparator*. Whenever $v_{in} > 0$, the op-amp output v_{out} will go to its negative limit (saturation); when $v_{in} < 0$, v_{out} will go to its positive limit. This is an *inverting* comparator, since v_{in} is connected to the op-amp's *–Input*.

Comparator-type circuits are useful in a variety of situations. For example, consider the circuit at right, where instead of grounding the *+Input*, it is connected to a constant *threshold* voltage source, V_{th} (shown here as a battery, but it could come from a user potentiometer setting or other voltage divider using the circuit power supplies, etc.). Whenever $v_{in} < V_{th}$ by a couple of millivolts or more the op-amp output is at positive saturation (V_{sat+}) and the LED is off. If v_{in} rises above V_{th} then the op-amp output goes to negative saturation (V_{sat-}) and the LED is illuminated. Such a circuit could, for example, warn an operator of excessive temperature or pressure if v_{in} is generated by an appropriate sensor.

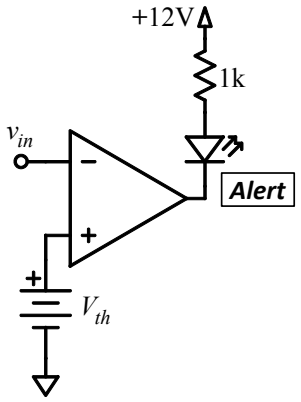
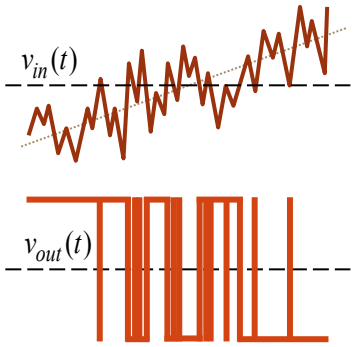


Figure 4-2: Inverting comparator used to illuminate a warning LED whenever $v_{in} > V_{th}$.

Another application could be to interface the output of the comparator circuit in Figure 4-1 to a digital system in order to count zero crossings of the input signal, perhaps to determine the input signal's frequency or to count the number of events detected by a sensor. Unfortunately, if there is significant noise in the input signal v_{in} as its average value slowly

rises through zero, many output transitions could be generated by the noise fluctuations while v_{in} is near V_{th}, as shown in Figure 4-3. Such behavior would render the circuit useless for a counting application.

Figure 4-3: One potential problem with the basic op-amp comparator shown in Figure 4-1: a slowly rising, noisy input can cause many closely-spaced output transitions as it passes through 0, as shown at right. This is undesirable if you need to use the circuit to accurately count zero-crossings of the underlying input signal.



Using positive feedback to add hysteresis*: the Schmitt trigger*

A common solution to the problem just outlined is to add *noise immunity* to the comparator circuit by incorporating *hysteresis* into its transition threshold voltage V_{th}, as shown in Figure 4-4. By "hysteresis" we mean that the threshold voltage is a function of the system's current *operating state*, which is defined for this circuit by its output voltage: positive or negative saturation (V_{sat+} or V_{sat-}). V_{th}, the voltage to which v_{in} is compared, is determined from the op-amp's v_{out} by a voltage divider constructed from resistors R_1 and R_2. V_{th} therefore changes in response to a change in the output voltage: when the output goes to positive saturation in

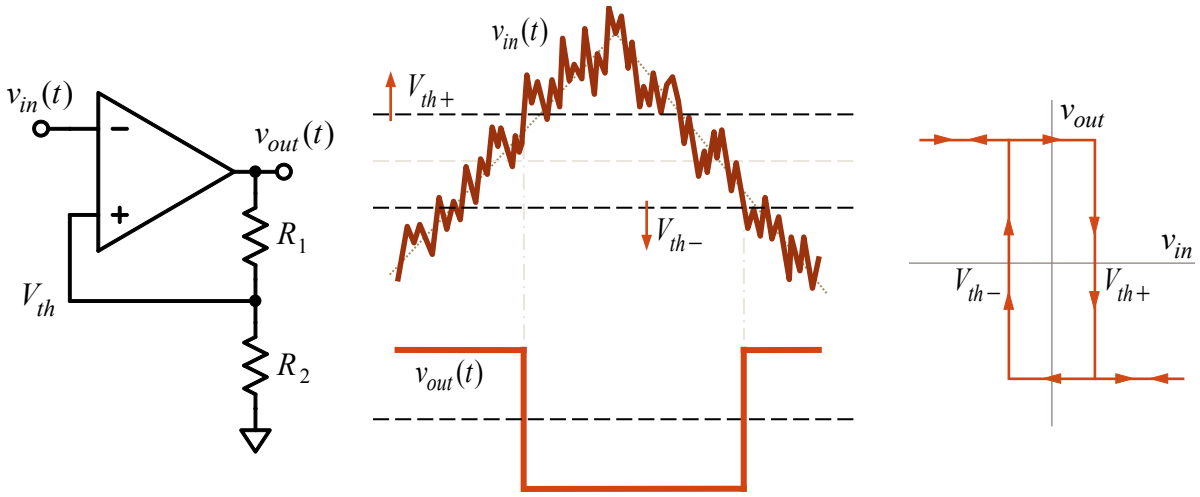


Figure 4-4: An inverting *Schmitt trigger* circuit, where positive feedback is used to add *hysteresis* to the comparator's transition threshold voltage. When the comparator's output is high the threshold voltage $V_{th+} > 0$, but when its output is low then $V_{th-} < 0$. The center plot shows how these differing thresholds can provide *noise immunity*: if $(V_{th+} - V_{th-})$ > [noise peak-peak amplitude], then as v_{in} slowly passes through 0 its noise fluctuations will be too small to trigger unwanted transitions in the output. The right-hand plot graphs the resulting *hysteresis loop* defining the relationship between v_{out} and v_{in}.

response to v_{in} passing below what was then the threshold voltage, V_{th} changes to a higher value (V_{th+}); conversely, an input voltage climbing through V_{th+} will change the output to its negative saturation state and cause the threshold voltage to be set to a lower value (V_{th-}), as illustrated in Figure 4-4.

As shown in the figure's middle graphic, this difference in V_{th+} and V_{th-} means that once a transition is triggered by a change in v_{in}, small noise excursions in the input will not cause v_{in} to reverse its course enough to cross back through the circuit's *hysteresis gap* ($V_{th+} - V_{th-}$) and cause an undesired reversal of the output state. If the hysteresis gap is made large enough, then the system can be made completely impervious to the noise in the input signal, eliminating the spurious output transitions suffered by the basic comparator circuit (Figure 4-1). Of course, the hysteresis gap should not be made so large that the interesting variations in v_{in} are too small to trigger a change in the circuit's output!

There happens to be another important advantage to the use of positive feedback in the comparator circuit of Figure 4-4: as the output changes, the positive feedback of v_{out} increases the difference between the op-amp's + and − input terminal voltages, accelerating the change in the output even if the op-amp's open-loop gain $g(\omega)$ is relatively modest. Because of the positive feedback, *the output voltage will change at an exponentially increasing rate* until the op-amp *slew rate limit* is reached, even if the initial difference between v_{in} and V_{th} is very small, or v_{in} is changing very slowly (slew rate is discussed in the next section). This "pulling oneself up by one's own bootstraps" effect is why positive feedback is also referred to as *regenerative feedback*. This idea of using regenerative feedback to incorporate noise immunity and to vastly increase output transition (*switching*) speed was first developed by Otto Schmitt in 1934 at Washington University (St. Louis, Missouri) using vacuum tube technology; consequently, a circuit incorporating these two features (threshold hysteresis and positive feedback) is called a *Schmitt trigger*. His invention has since been almost universally applied in the design of modern, high-speed digital circuitry.

Op-amp slew rate limitations

Just how fast can an op-amp's output voltage change in response to a nonzero difference in the voltages at its two inputs ($v_+ - v_-$)? In Experiment 2 you examined the real op-amp's finite *frequency response*, as captured in its gain-bandwidth product f_{BW}. If you look back at our cartoon model of the ideal op-amp in Experiment 1 (Figure 1-14 on page 1-12), you can think of an op-amp's frequency response limitation as analogous to a finite "reaction time" on the part of the little technician controlling the op-amp's output voltage — the technician can't quite keep up with rapid oscillations in $v_+ - v_-$, so the op-amp's output gets smaller and is delayed in phase as the input frequency increases.

In addition to its frequency response there is another, unrelated limit to an op-amp's speed: its output *slew rate* limit. To relate this limitation to our little technician's performance, slew rate describes how fast he can *change the output voltage* once he notices that it needs to be changed. Slew rate is specified in volts/μsec and comes into play when large swings in the output voltage are required, as for comparator applications. The slew rate of the TL082 is specified to be at least 8 V/μsec and is typically 13 V/μsec. Its effect is demonstrated in Figure 4-5.

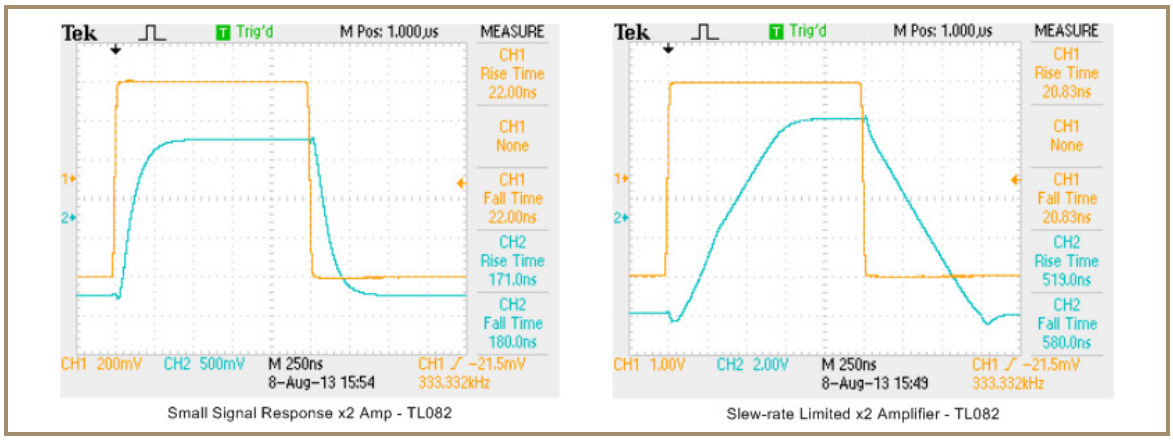


Figure 4-5: Oscilloscope recordings of the response to a square wave input (orange trace) of a gain 2 noninverting TL082 op-amp amplifier. The output (blue trace) at left changes by only 2V with each step and is limited by the ×2 amplifier's bandwidth of about 1.5 MHz. As you can see, it responds to an input step with an exponential relaxation with a time constant $\tau \approx 100$ns, as expected. In the right image the input is 5 times larger (5V vs. 1V), so the output must now change by 10V with every input step. Note that the output now changes at a nearly constant rate during these steps, so that the output waveform shape is *qualitatively different* from the left-hand image. The right-hand output is *slew rate limited*: the slope is about 2V/150ns ≈ 13V/μs, as specified in the manufacturer's data sheet.

Unlike the effect of finite frequency response, slew rate limiting is an example of a *nonlinear effect* on the amplifier's output. Linear effects aren't qualitatively affected by the size of the input, but clearly, in this case, size *does* matter (the output waveforms in the right and left images in Figure 4-5 are *qualitatively* different).

Schmitt trigger circuit variations and trigger point calculations

Calling the op-amp positive and negative output saturation voltages V_{sat+} and V_{sat-}, the resulting hysteresis gap for the circuit of Figure 4-4 is:

4.1
$$V_{th+} - V_{th-} = \frac{R_2}{R_1 + R_2}\left(V_{sat+} - V_{sat-}\right) \qquad \textbf{(inverting)}$$

For the TL082 with ±12V power supplies, the magnitudes of V_{sat+} and V_{sat-} are very slightly different, and $V_{sat+} - V_{sat-} \approx 21\text{–}22\text{V}$. Because the bottom of R_2 in Figure 4-4 is connected to ground, the threshold voltages V_{th+} and V_{th-} will be centered around 0V (assuming that $V_{sat-} = -V_{sat+}$). Connecting the bottom of R_2 to a voltage source differing from ground *will not affect the width of the hysteresis gap*, but it will center that gap around a nonzero mean threshold proportional to the applied reference voltage V_{ref} (see Figure 4-6 and equation 4.2).

4.2 $$\overline{V_{th}} = \tfrac{1}{2}\left(V_{th+} + V_{th-}\right) = \frac{R_1}{R_1 + R_2} V_{ref} \qquad \textbf{(inverting)}$$

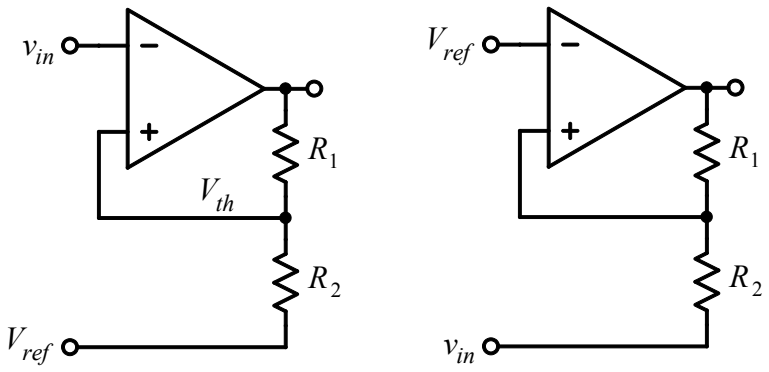
A noninverting Schmitt trigger may be implemented by simply swapping its input and reference voltage connections (Figure 4-6), but now the formulas for the threshold voltages are different from those for the inverting case, because now the voltage divider affects v_{in} rather than V_{ref}:

4.3 $$V_{th+} - V_{th-} = \frac{R_2}{R_1}\left(V_{sat+} - V_{sat-}\right) \qquad \textbf{(noninverting)}$$

4.4 $$\overline{V_{th}} = \tfrac{1}{2}\left(V_{th+} + V_{th-}\right) = \frac{R_1 + R_2}{R_1} V_{ref} \qquad \textbf{(noninverting)}$$

Additional Schmitt trigger circuit design considerations

Note that equation 4.3 places an important restriction on the ratio R_2/R_1 for a noninverting Schmitt trigger: unless $R_2 < R_1$, the hysteresis gap ($V_{th+} - V_{th-}$) will exceed the output voltage swing range of the op-amp ($V_{sat+} - V_{sat-}$), and, depending on the reference voltage value V_{ref}, *one or both of the Schmitt trigger thresholds will be beyond the range of an op-amp's output*



Inverting *Noninverting*

Figure 4-6: Inverting and noninverting Schmitt triggers with a supplied reference voltage V_{ref} used to set the trigger thresholds. Note that the voltage source connected to the bottom of R_2 in each circuit must have an output impedance « R_2 or the trigger points will be affected because of the current flowing between the op-amp's output and that source.

voltage. Assuming that the input signal voltage range is limited to be between V_{sat+} and V_{sat-}, the circuit's output could experience *lock-up* at V_{sat+} or V_{sat-}, rendering the circuit useless!

For either circuit in Figure 4-6, it is also important to remember that the voltage source connected to R_2 must have a small output impedance, or that source's output impedance must be added to R_2 when calculating the trigger thresholds using equations 4.1 through 4.4. If necessary, use a voltage follower between the source and R_2.

Another design consideration is the current required from the op-amp output to drive the voltage divider formed by resistors R_1 and R_2. As the total feedback resistance $R_1 + R_2$ is reduced, then the additional current drawn by them may cause significant changes in the op-amp's behavior, and the circuit will not work as you expect. If, say, both are chosen to be 1 k, then their series resistance is 2k. When the op-amp output is at saturation (approx. ±11V), then over 5 mA will be required from the op-amp output. This relatively large current draw could reduce the TL082 op-amp's saturation voltages to only about ±9V, as shown in its data sheet, also reducing the hysteresis between the Schmitt trigger threshold voltages.

THE RELAXATION OSCILLATOR

Simple, one op-amp oscillator

If you feed the output of an inverting Schmitt trigger circuit back to its input through a *RC* voltage divider, you get a circuit whose output switches back and forth between the op-amp's two saturation limits: you have made a simple *relaxation oscillator* (Figure 4-7).

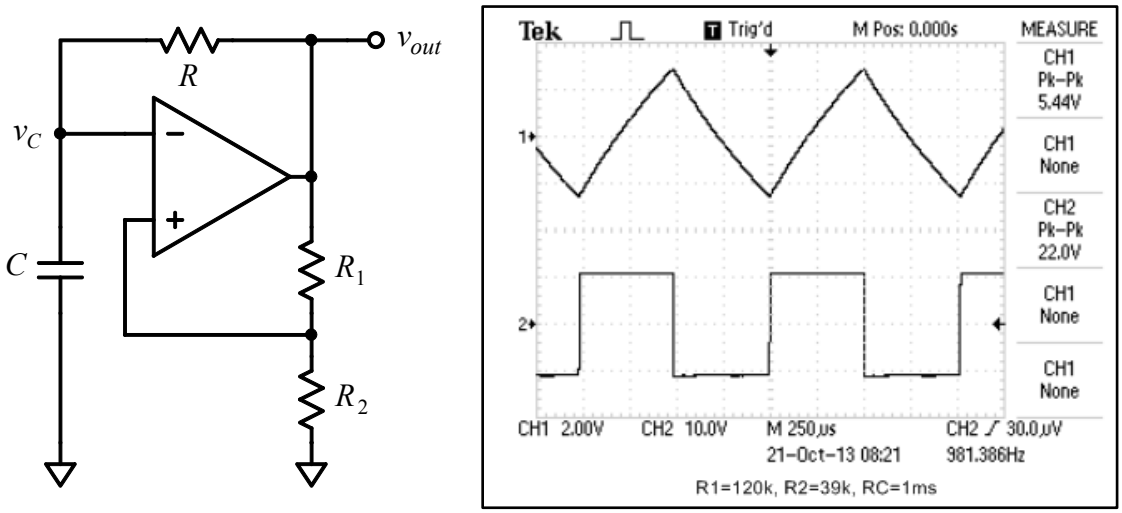


Figure 4-7: A simple *relaxation oscillator* using a Schmitt trigger to alternately charge and discharge the capacitor *C* through the resistor *R*. Whenever v_C, the voltage across *C*, reaches a trigger threshold, the op-amp output voltage reverses to its opposite saturation limit. Thus the current through *R* changes sign, and the capacitor voltage moves toward the opposite threshold. Consequently, v_C oscillates between the Schmitt trigger's two threshold voltages as the op-amp output switches back and forth between its two output saturation limits. The oscilloscope image shows v_C (CH1) and v_{out} (CH2) for trigger thresholds chosen so that $f = 1/RC$.

As should be clear from the figure, the op-amp's output charges the capacitor *C* via a current supplied through resistor *R*. Because the capacitor's voltage is monitored by the op-amp's *–Input*, every time the voltage on *C* crosses a trigger threshold (the fraction of V_{sat} applied to the op-amp's *+Input*) the op-amp output switches to its opposite saturation voltage, changing the direction of the current through *R*. Thus the capacitor voltage then begins to move toward the new op-amp output voltage. Each op-amp output voltage change also changes the sign of the voltage at the op-amp's *+Input*, however, and the op-amp output will again change state when the capacitor's voltage reaches this opposite threshold. The process repeats indefinitely as shown by the oscilloscope screen image in Figure 4-7.

The capacitor's voltage profile is a sequence of exponential relaxations toward the op-amp's alternating output saturation voltages, $\pm V_{sat}$, each relaxation interrupted when a threshold is reached. If the + and – saturation voltages are assumed to be equal, then each exponential relaxation is described by (changes sign with each op-amp output transition):

$$v_C(t) = \pm\left[V_{sat} - (V_{sat} + V_{th})\,e^{-t/RC}\right] \qquad 4.5$$

To determine the oscillation period T, note that after each half-period the capacitor voltage reaches the next trigger threshold, so the expression inside the brackets in (4.5) goes from $-V_{th}$ at $t = 0$ to $+V_{th}$ at $t = T/2$. With equation 4.1 relating the inverting Schmitt trigger circuit's V_{sat} and V_{th}, the relationship between the period T and the circuit's component values is:

$$\frac{R_1}{R_2} = \coth\left(\frac{T}{4RC}\right) - 1 \qquad \textbf{4.6}$$

where **coth** is the hyperbolic cotangent function. For example, if you want the oscillator period to equal the filter's RC time constant ($T = RC$), then $R_1 = 3.08\,R_2$. Choosing the pair of standard resistor values $R_1 = 120\,\text{k}$ and $R_2 = 39\,\text{k}$ provides a close match to this ratio (within 0.2%).

Note that the op-amp output must supply a current to the capacitor as high as $(V_{sat} + V_{th})/R$ just after the op-amp output changes state — excessive current here will reduce V_{sat} as the op-amp tries to meet this output current requirement, distorting the output waveforms and lengthening T. Choosing $R \geq 10\,\text{k}$ should limit the capacitor charging current to a reasonable level.

Function generator

Modifying the above relaxation oscillator to charge the capacitor with a constant current would then cause the capacitor's voltage to change at a constant rate rather than with an exponential relaxation. This may be accomplished by using an op-amp integrator rather than the simple RC pair of Figure 4-7; the resulting circuit is shown in Figure 4-8. In the figure op-amp U1 along with its R and C form the integrator, which is just an inverting amplifier

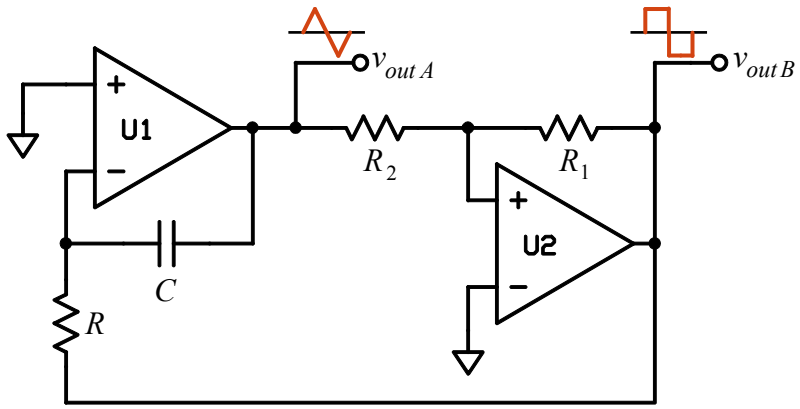


Figure 4-8: Integrator U1 coupled to Schmitt trigger U2 to form a simple *function generator*, outputting triangle and square waveforms. Since the integrator is inverting, its output must go to a noninverting Schmitt trigger, so that reaching a trigger point reverses the capacitor's charging current. This means that we must have $R_1 > R_2$, or the circuit won't work.

with C as its feedback element.[1] The input to R is the alternating saturation voltage of the noninverting Schmitt trigger composed of U2, R_1, and R_2.

Because op-amp U1's *–Input* will be a virtual ground (equal to its grounded *+Input*), the voltage across R will be U2's $\pm V_{sat}$ output, and the current through R will be $\pm V_{sat}/R$. This must also be the current through the capacitor C, alternately charging and discharging it as op-amp U2's output changes sign:

4.7
$$\frac{d}{dt} v_C(t) = I_C(t)/C = \pm V_{sat}/RC$$

Since the voltage at the junction of R and C is 0 (a virtual ground), U1's output voltage will be $-v_C(t)$. This means that U1's output voltage is a nice, linear ramp, going in a direction opposite to the polarity of U2's saturation voltage. As this output reaches a threshold voltage of the Schmitt trigger (U2, R_1, and R_2), it reverses U2's saturation voltage, reversing the current through the integrator's R and C. U1's output voltage then ramps the other way until it reaches the Schmitt trigger's opposite threshold, repeating the process.

Thus the output of U1 in Figure 4-8 is a symmetric triangle-wave whose peak voltages are the Schmitt trigger's threshold voltages, $\pm(R_2/R_1)\,V_{sat}$ (from equation 4.3). As mentioned in the caption of Figure 4-8, we must use the noninverting form of the Schmitt trigger because the integrator is inverting. Because U1's output will have a constant slope between triggers, the oscillation period is much easier to calculate for this circuit; the formula is left to the exercises.

Figure 4-9 on page 4-10 shows a circuit which incorporates both variable frequency and variable symmetry adjustments to the output waveforms. Note how the diodes select which side of the symmetry potentiometer is used to set the current through the integrator's capacitor (depending on the sign of U2's output). The voltage follower (U3) isolates the Schmitt trigger's square wave output and its frequency adjust potentiometer from the current load required by the integrator, so changing the symmetry potentiometer setting will not affect the voltage divider ratio set by the frequency potentiometer or op-amp U2's output saturation voltages.

Figure 4-9 presents one of the most complicated circuits we've considered so far. You should spend some time studying this circuit so that you understand how it works and how you would select values for the components (the prelab exercises will help you focus on this task!). Why is the resistor in series with the output of op-amp U3 necessary? You will design a circuit which replaces the frequency adjust potentiometer and its associated U3 voltage follower with a multiplier in order to set the function generator's frequency using a control voltage input.

[1] The op-amp integrator circuit is described in greater detail in Experiment 2. Equation 2.27 on page 2-35 describes the relationship between the integrator's output and input voltages. The function generator's overall feedback via the Schmitt trigger avoids the saturation problems of the simple integrator circuit described in Experiment 2, eliminating the need for the extra resistor R_{DC} used in the Experiment 2 integrator design.

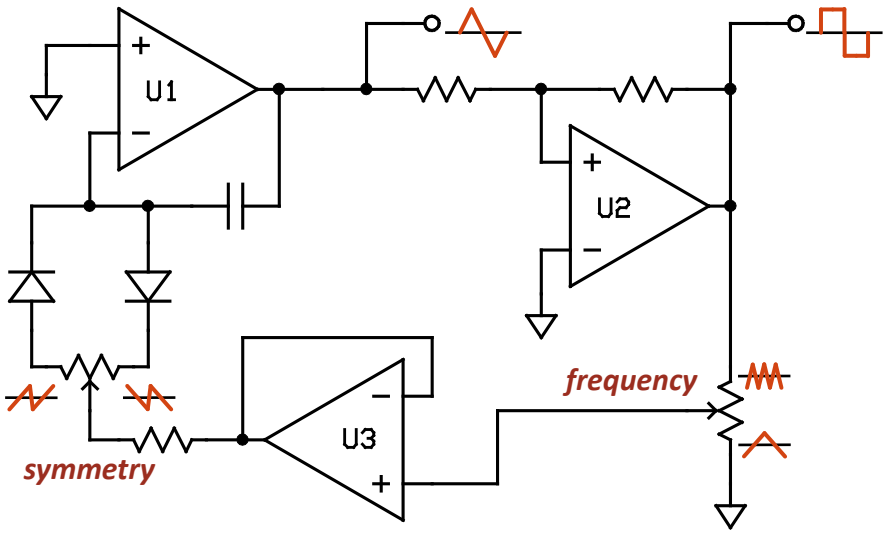


Figure 4-9: A function generator circuit with variable frequency and waveform symmetry. The voltage follower using op-amp U3 isolates the Schmitt trigger output and its frequency adjust potentiometer from the current load demands of the integrator, especially important when the symmetry potentiometer is set near one of its limits.

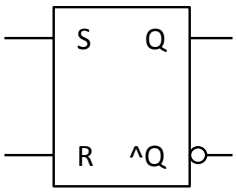
THE 555 TIMER AND MULTIVIBRATOR CIRCUITS

Introduction

Next we consider a special integrated circuit designed specifically for timing and oscillator applications: the *555 timer IC*, invented in 1971 by Hans R. Camenzind while working for *Signetics* (since absorbed into *NXP Semiconductors*). The version you will use for this experiment is the TLC555, an updated version manufactured by Texas Instruments. They and other companies also manufacture copies of the original version: for example, the LM555, produced by Fairchild (now part of ON Semiconductor). The LM555 data sheet gives a very few examples of the sorts of circuits you can build using this versatile device; a more thorough discussion of the device and its applications is provided in the original Application Note. Interestingly, *Wikipedia®* claims that the 555 timer is the most popular IC ever made — selling, for example, over a billion units in 2003 alone. The 555 timer is an example of a *mixed signal* or *interface* IC, incorporating both analog and digital circuitry. Before describing its operation in detail, we will first examine its digital element, a so-called *RS flip-flop*.

The RS flip-flop

The heart of the 555 timer IC is its *RS* (*R*eset-*S*et) flip-flop: a type of digital circuit which determines the *operating state* of the device. The schematic logic symbol and operation of a generic *RS* flip-flop are diagrammed in Figure 4-10. A *flip-flop* is the generic term designers use for a two-state digital element which changes its operating state only when some particular sequence of input signals is encountered; otherwise it remains in its current state. In other words, a flip-flop is an elementary, 1-bit digital *memory*. As shown in Figure 4-10, our flip-flop has two inputs: *Set* (S) and *Reset* (R). A binary logic 1 (*true*) applied to one input



S (set)	R (reset)	Q (output)
0	0	unchanged
1	0	1
0	1	0
1	1	undefined*

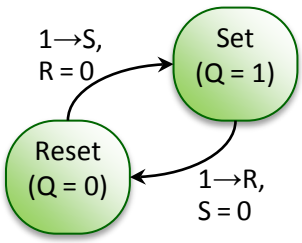


Figure 4-10: A generic *RS* flip-flop and its operation. Inputting a logic 1 to either one of the two terminals S or R determines the Q output terminal's logic state as shown by the logic table and the state diagram; the ^Q terminal's output state will assume the opposite of Q's state (0 if 1, 1 if 0). While both inputs are held at logic 0, the Q and ^Q output terminal values will be maintained.

*** Although the behaviors of the Q and ^Q outputs of a generic RS flip-flop are undefined when both the S and R inputs are logic 1 at the same time, the 555 timer IC flip-flop gives precedence to its S input, setting Q to 1 and ^Q to 0.**

drives the *RS* flip-flop to its corresponding operating state: *Set* (Q = 1; ^Q = 0) or *Reset* (Q = 0; ^Q = 1). Unlike the case for a generic *RS* flip-flop, if both inputs are logic 1 at the same time the 555 flip-flop gives priority to its S input. The flip-flop then maintains its established state as long as the inputs are both 0.

555 timer operation

Figure 4-11 shows a functional block diagram and the device *pinout* for the complete 555 timer IC, which at first glance seems very complicated. Let's start with its power supply terminals: *V+ Power* and *Ground*. The TLC555 device's recommended power supply voltage range is +2V to +15V (with respect to its ground terminal). **All input voltages to the 555 must remain between the values established by *V+ Power* and *Ground*!**

The 555's internal *RS* flip-flop figures prominently in determining its behavior. The flip-flop's operating state sets the condition of the two 555 output terminals, *Output* and *Discharge.* Its *R* and *S* inputs in turn come from comparators which monitor the voltages on the 555's *Threshold* and *Trigger* inputs, respectively. The reference voltages for these comparators come from a three-resistor voltage divider between the IC's power supply and ground. In the original 555 IC, these resistors all have values of 5 k, so that the reference voltages will be 2/3 and 1/3 of the power supply voltage. In the TLC555 the common value of the three "resistors" is unspecified by its data sheet but should be around 100 k.[2]

The 555 *Discharge* terminal can be either in a high impedance state (*off*) or connected to the 555's ground terminal (*on*, *shorted*), as indicated by the switch in the functional diagram. As

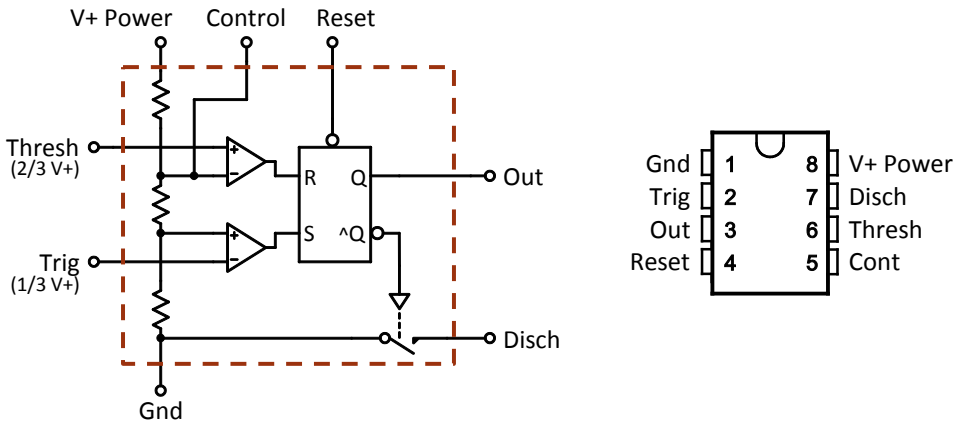


Figure 4-11: The *555 Timer* IC. Shown are both its functional block diagram and the IC *pinout*, or pin numbering scheme and identification. The heart of the circuit is its *RS flip-flop* whose operating state determines the 555 outputs *Out* and *Disch*. Voltages at the *Thresh* and *Trig* inputs are used to trigger two analog comparators which in turn control the flip-flop's state.

[2] Legend has it that the original 555 IC got its designation from its three 5k resistors, but Wikipedia® disputes this claim. In the TLC555 the three are not resistors at all, but three pairs of MOS (metal-oxide-semiconductor) transistors emulating large-valued resistors.

its name suggests, this terminal's purpose is to periodically discharge an external timing capacitor used with the 555. The IC also has a separate *Reset* terminal input (see Figure 4-11) which overrides any other command to its internal flip-flop and drives it to its *Reset* state (the little circle on the wire from the *Reset* input at the top of the flip-flop in means that it is active when its input is *Low*: a 0V input commands the flip-flop to *Reset*; otherwise the pin should be connected to *V+ Power* to inactivate it.). Finally, the *Control* pin can be used to directly adjust the threshold and trigger reference voltages in order to modulate the timing of the IC's output signal.

The following state table itemizes the possible input combinations and how they affect the 555 output terminals.

Table 4-1
555 Timer State Table

Reset (pin 4)	Trigger (pin 2)	Threshold (pin 6)	Output (pin 3)	Discharge (pin 7)
high	*LOW (< 1/3 V+)*	-	*HIGH (near V+)*	*OPEN (off)*
high	high	low	no change	no change
high	high	*HIGH (> 2/3 V+)*	Low (near Gnd)	Short to Gnd (on)
LOW (< 0.4V)	-	-	Low (near Gnd)	Short to Gnd (on)

The *ACTIVE* state of each input is highlighted with italics, as shown. The *Reset* input (active when *LOW*) overrides all other inputs; otherwise *Trigger* overrides *Threshold* when determining the flip-flop state. The active response state is *Output HIGH*, *Discharge OPEN*. Connect *Reset* to *V+ Power* (pin 8) if it is not used.

The normal sequence of events when using the 555 is as follows (the *Reset* pin is kept *high*):

1. The *Trigger* pin is brought *low*, setting *Output* to *high* and *Discharge* to *open.* The *Threshold* pin should also be *low*.
2. With the *Threshold* pin *low*, the *Trigger* is brought back to *high*; the outputs remain unchanged: *Output* is *high* and *Discharge* is *open*.
3. After some time, the *Threshold* is brought *high*, which resets the *Output* to *low* and shorts *Discharge* to ground.
4. Finally, *Threshold* is brought back *low*.

Let's now see how to use this event sequence to do something interesting…

Astable multivibrator (relaxation oscillator)

The first application of the 555 IC we consider, Figure 4-12 on page 4-14, is as an *astable multivibrator* (which is the name used for a relaxation oscillator by digital electronics

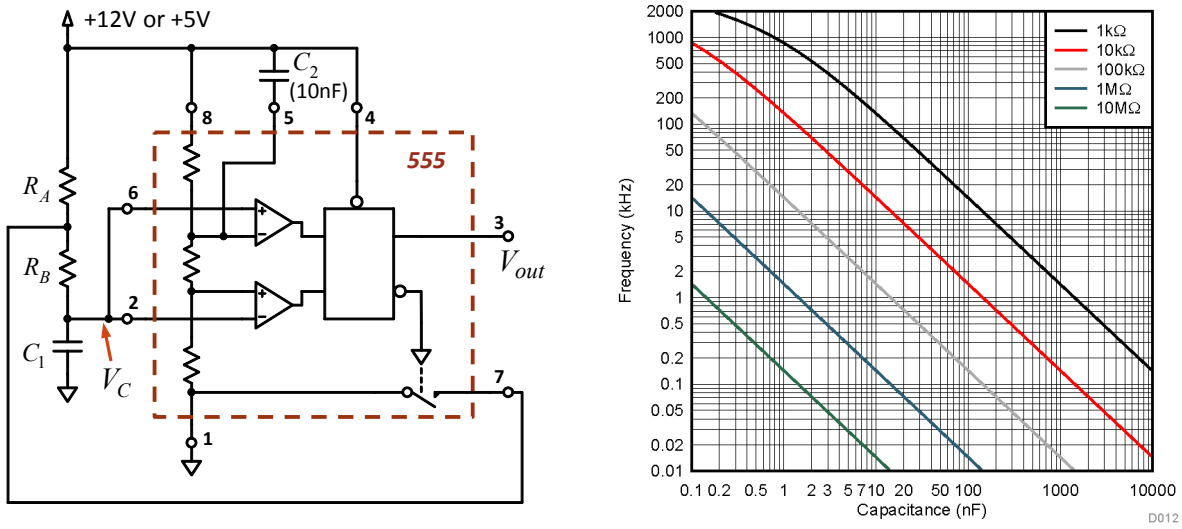


Figure 4-12: *Astable multivibrator* using the 555. The V_C and V_{out} waveforms are similar to those for the simple relaxation oscillator in Figure 4-7. The graph at right is from the TLC555 Data Sheet (Copyright © 1983–2019, Texas Instruments Incorporated); it shows how *total* resistance $R_A + 2\,R_B$ and capacitor selection affect the output frequency. IC pin numbers are shown next to the 555 terminals in the schematic.

engineers). The idea is to repeatedly charge and discharge a capacitor (C_1) while monitoring its voltage using the 555's *Trigger* and *Threshold* inputs. The capacitor will be charged using the system power supply voltage (V_{supply}) through resistors R_A and R_B; when the capacitor's voltage (V_C) reaches the *Threshold* reference ($2/3\ V_{supply}$), the flip-flop changes state and shorts the *Discharge* terminal to ground: this then discharges the capacitor through R_B. When V_C has discharged to the *Trigger* reference voltage ($1/3\ V_{supply}$), the 555's flip-flop again changes state, opening the *Discharge* terminal so that the capacitor again starts to charge, repeating the process.

Thus C_1's voltage V_C relaxes back and forth between $1/3$ and $2/3$ of the supply voltage with time constants $(R_A+R_B)\,C_1$ when rising and $R_B C_1$ when falling, so the oscillator period will be proportional to the resistance $R_A+2\,R_B$, use this sum when referring to the resistance curves in the graph accompanying the schematic in Figure 4-12. Because the capacitor's charging time constant is longer than its discharge time constant, the output waveform's *duty cycle* (ratio of high duration to the total period) will be greater than 50%.

> The TLC555 has very high impedance inputs for its *Trigger* and *Threshold* terminals, so large resistor values may be used to achieve very long oscillator periods; only about 10pA is drawn by either input terminal, and the leakage current into the *Discharge* terminal is only about 100pA when it is open. Oscillator periods of a few hours or longer are easily achievable.

When the *Discharge* terminal is shorted to ground, V_{supply} is applied across R_A, and this current will add to the capacitor's discharge current through R_B also flowing into the

Discharge terminal. Clearly, the values of R_A and R_B should be large enough (at least a few kΩ) to keep these currents from becoming excessive.

The 555's *Reset* and *Control* input terminals aren't needed for this application, but they can't be ignored. *Reset* (pin 4) should be tied to the 555's *V+ Power* (pin 8) so that noise will not cause spurious resets. Similarly, *Control* (pin 5) should be connected to pin 8 through a small capacitor $C_2 \sim 10\,\text{nF}$ to keep noise from affecting the comparators' trigger points.

Monostable Multivibrator (one-shot)

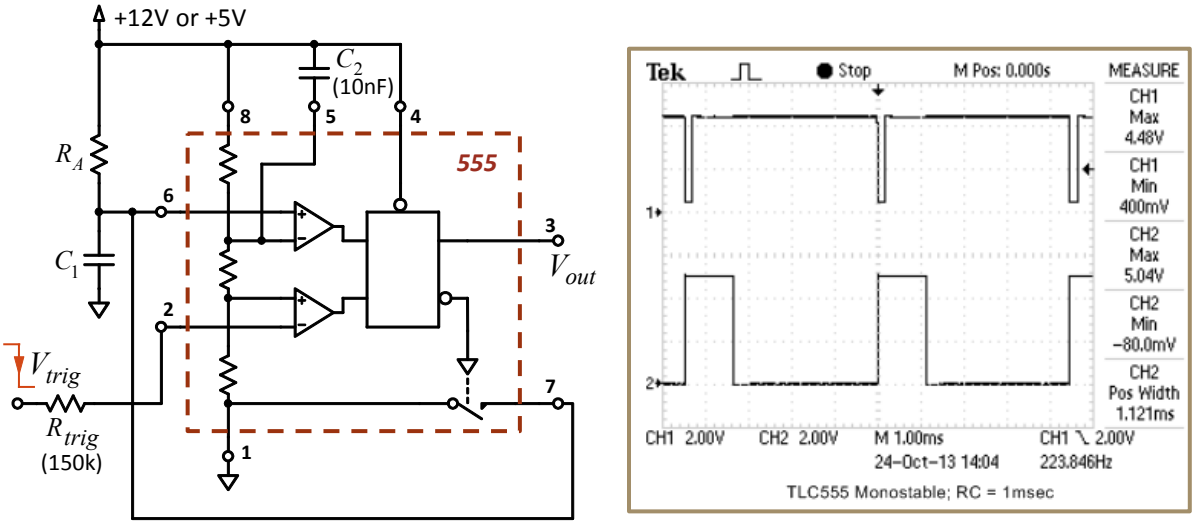


Figure 4-13: *Monostable multivibrator* using the 555. Whenever V_{trig} is brought below 1/3 V_{supply} the output goes high and capacitor C_1 starts to charge through resistor R_A. When the capacitor voltage reaches 2/3 V_{supply}, the output goes low, the *Discharge* terminal is shorted to ground, and C_1 is discharged back to 0. The oscilloscope shows trigger event inputs (CH1) and the resulting pulse outputs (CH2). Note that for proper operation, the trigger pulse input must be shorter than the resulting output pulse width.

Whereas neither the high nor the low output state of a relaxation oscillator is *stable* (because each state eventually changes to the other without any external input to the circuit), one of the states of a *monostable multivibrator* is stable — an external trigger input is needed to make the circuit transition to its other output state. The other state, however, is *unstable*: after some time the circuit will transition back to its stable state and remain there until another trigger event occurs. The idea is that a trigger event causes the circuit to emit a single pulse of a fixed width and then return to its original, quiescent state. For this reason the monostable multivibrator is also called a *one-shot*: one output pulse for each input trigger.

Figure 4-13 (above) shows how to implement a simple one-shot using the 555 timer. Assume the capacitor C_1 is discharged and the 555's *Trigger* input voltage (V_{trig}) is greater than 1/3 of the power supply voltage (V_{supply}). Assume further that the 555 is in its *Reset* state

($V_{out} = 0$ and the *Discharge* terminal shorted to ground). This is the circuit's *stable* (quiescent) state.

A *trigger event* occurs when V_{trig} is momentarily taken well below $1/3\,V_{supply}$. Now the 555 transitions to its active state: the *Discharge* terminal opens and V_{out} goes high. The capacitor then charges through R_A toward V_{supply}; when its charge reaches $2/3\,V_{supply}$, the 555 *Threshold* is triggered. If before this happens V_{trig} has been returned to its quiescent state (well above $1/3\,V_{supply}$) then the 555 will return to its *Reset* state, lowering V_{out} and discharging the capacitor back to ground. The time it takes the capacitor voltage to relax from 0V to $2/3\,V_{supply}$ is just over one time constant, i.e. $\approx 1.1 R_A C_1$.

Note that if the trigger input voltage remains below $1/3\,V_{supply}$, then the 555 will remain in its active state (V_{out} high), since the *Trigger* comparator overrides the *Threshold* comparator (see Table 4-1 on page 4-13). If the capacitor voltage has exceeded $2/3$ of V_{supply}, then as soon as V_{trig} goes back above $1/3\,V_{supply}$ the 555 will change state, and its output will immediately return to 0.

The IC's *Trigger* input (pin 2) is protected against excessively low or high V_{trig} voltages ($V_{trig} < 0$ or $V_{trig} > V_{supply}$) by the resistor $R_{trig} = 150\,\text{k}$. This resistor limits the current flow within the 555 IC during these V_{trig} excursions so that the 555 isn't permanently damaged.

As with the astable multivibrator circuit, input signals to the 555's Reset and Control pins aren't required for this application, so properly connect them as described before (as in Figure 4-12 and Figure 4-13).

Additional 555 applications

So far we have just scratched the surface of the many applications of the 555 IC. Many more are described in the LM555 datasheet and the 555 Application Note. The web, of course, has sites with myriads of circuits; check out http://www.555-timer-circuits.com.

PRELAB EXERCISES

1. Consider the function generator circuit in Figure 4-8 on page 4-8. Sketch the waveform at op-amp U2's +*Input* terminal.

2. Use equations 4.3 on page 4-5 and 4.7 on page 4-9 to show that the oscillation period T of the simple function generator circuit in Figure 4-8 is given by:

4.8

$$T = 4RC\left(R_2/R_1\right)$$

Will the circuit work if $R_2 > R_1$ (consider equation 4.3)? What should be the generator frequency f if $R = 10\,\text{k}$, $C = 0.1\,\mu\text{F}$, $R_1 = 10\,\text{k}$, and $R_2 = 1\,\text{k}$? What is the output amplitude (peak-to-peak) of the triangle wave output at U1 if the square wave amplitude output at U2 is 22V peak-to-peak?

3. How does the symmetry control potentiometer in Figure 4-9 on page 4-10 affect the output waveform symmetry (how does this part of the circuit work)? Does it change the output frequency by any significant amount when it is adjusted? If the magnitude of the maximum output current available from an op-amp is 10mA and the magnitude of its saturation voltage is 11V, then what is the minimum allowable value for the resistor in series with the output of op-amp U3 for the circuit to work properly?

   How does the frequency control potentiometer in Figure 4-9 affect the output frequency? Does it affect the waveform symmetry to any significant degree when it is adjusted?

4. Consider the monostable multivibrator circuit in Figure 4-13 on page 4-15. Sketch the voltage waveform at the 555 IC pin 6 (its *Threshold* terminal) to accompany the trigger voltage and output voltage waveforms shown in the oscilloscope screen shot.

5. Return to the function generator circuit in Figure 4-8 on page 4-8. How could you add a multiplier (using the MPY634) to that circuit to provide an input so that an applied voltage will determine the function generator's frequency? Such a circuit is called a *VCO* for *voltage-controlled oscillator*.

   Design a circuit which will output a frequency proportional to the input control voltage applied to the circuit such that half the original circuit frequency ($1/T$, where T comes from equation 4.8 above) will be generated when the control voltage is $\approx 5\text{V}$ (it's ok if the circuit cannot quite generate a frequency as high as $1/T$, since the multiplier output will be $< 10\text{V}$). Provide a complete schematic of your circuit using the component values supplied in problem 2 above and assigning values to any additional components you might add.

   Are there limits to the input control voltage beyond which the circuit stops working?

LAB PROCEDURE

Overview

During lab you will investigate the behavior of a Schmitt trigger circuit and measure its hysteresis and its op-amp's slew rate. You will then look at a couple of relaxation oscillator circuits, including the circuit you designed in response to Prelab exercise problem 5.

Next you will build an astable multivibrator circuit using a TLC555 timer IC. To accomplish this task you will need to construct the circuit in the breadboard area of the analog circuit trainer, including installing the integrated circuit and correctly wiring to its pins. This will help prepare you for your upcoming project work, which will be built completely on such a breadboard. ***Make sure you pay attention to the clock during lab and budget enough time to complete this work!***

The Schmitt trigger and op-amp slew rate

Build an inverting Schmitt trigger (Figure 4-4 on page 4-2) using one of the op-amps on the analog trainer which have installed resistors available on its *+Input*. Using a triangle-wave input signal, measure its trigger thresholds V_{th+} and V_{th-}. Briefly note how these thresholds change when you change the feedback resistor values. See if you can use the **XY** display mode of the oscilloscope to generate a hysteresis plot like the center image in Figure 4-4.

Return the oscilloscope to its **YT** display mode. Input a 100 kHz square-wave signal to your Schmitt trigger. Expand the oscilloscope's horizontal time resolution around one of the op-amp output transitions. Does the transition resemble that in the right-hand image of Figure 4-5 on page 4-4? Estimate the op-amp's slew rate.

Function generator

Construct the function generator circuit shown in Figure 4-8 on page 4-8. With installed resistor and capacitors available on the trainer, use the component values listed in Prelab exercise problem 2. Take an oscilloscope screen shot showing the both the triangle and square waveform outputs. Does your oscillator's frequency *f* and its triangle wave amplitude agree with your solution to problem 2?

Voltage-controlled oscillator (VCO)

Using your solution to Prelab problem 5, add a multiplier to your function generator circuit to convert it to a *VCO*. Test its performance using the signal generator to generate a constant DC voltage for your circuit's frequency control input (your TA or the lab instructor can show you how to set up the signal generator).

Next use a low-frequency sine wave signal generator output (with an appropriate amplitude and **DC offset**) to modulate the output frequency of your VCO. Trigger the oscilloscope from

the signal generator's voltage to your VCO and take a screen shot showing this control voltage along with your VCO output. This sort of modulation is called *frequency modulation* (FM).

Building a TLC555 timer circuit

Warning

Do not connect the breadboard circuit to the analog trainer power supply until either your TA or the course instructor has looked over your circuit. Wiring the power supply incorrectly into an integrated circuit will often leave it fatally damaged.

Construct the astable multivibrator circuit (Figure 4-12 on page 4-14) in the breadboard area of the trainer. Your TA or the course instructor will give you a TLC555 IC and show you how to determine its pin numbers. Make sure you understand how the various contacts of the breadboard are interconnected and pay attention to the advice your TA and the course instructor give you regarding the layout and wiring of your circuitry on the breadboard.

Caution

555 Timer Voltage Limits

The maximum allowable voltage difference between the *V+ Power* and *Ground* terminals is ***less than 16V*** or so (depending on the specific IC version). Always connect the *Ground* terminal to the breadboard ground; you may then use +12V or +5V for *V+ Power*.

Never let a terminal voltage exceed the limits set by *Ground* and *V+ Power*! In particular, ***never let an input signal go < 0V (Ground)***. Violating this rule means nearly instant destruction of the IC. For the TLC555, putting a 150 kΩ resistor in series with an input should protect the IC from inadvertent inputs between +12V and −12V, regardless of its power supply voltage values.

Pick component values which will give an output frequency of a couple of kilohertz. Use at least 10 kΩ for resistor R_A to avoid excessive current draw when the capacitor C_1 is being discharged. Using the +12V power supply for V_{supply}, observe the capacitor voltage V_C and the output voltage V_{out}. Does the output change state when $V_C = 4\text{V}$ and 8V? Take a screen shot; compare your circuit's output frequency to the chart included with Figure 4-12.

Now use +5V as the power supply voltage (available from a connector on the front of the trainer). Does the output frequency change by very much from what it was with the 12V supply?

Additional circuits

If you have time, reconfigure your 555 circuit as a monostable multivibrator (Figure 4-13 on page 4-15). Don't forget the 150 k resistor R_{trig} to protect the IC's *Trigger* input from errant trigger voltage inputs!

You can use the pulse output of the signal generator as a trigger source: set the pulse **HiLevel** to about $0.9V_{supply}$ and its **LoLevel** to 0V. Set the **Dty Cyc** to ≈90% or more to generate a narrow, negative-going pulse as in the oscilloscope image in Figure 4-13. Try to capture a result similar to the result in that figure.

If you have time, look for circuits to try in the *More circuit ideas* section or in the 555 Application Note.

Lab results write-up

As always, include a sketch of the schematic with component values for each circuit you investigate, along with appropriate oscilloscope screen shots. Make sure you've answered each of the questions posed in the previous sections.

MORE CIRCUIT IDEAS

An edge to pulse converter

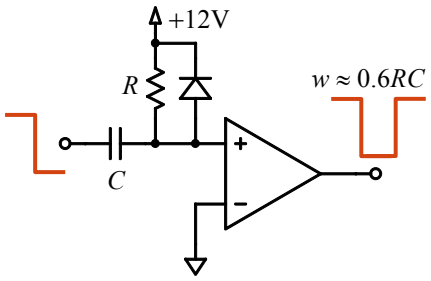


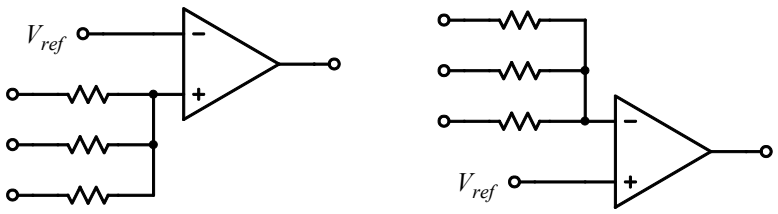
Figure 4-14: This circuit can output a narrow pulse for every high-to-low transition at its input.

The comparator circuit at right will take a falling input transition (edge) from V_{sat+} to V_{sat-} and output a short, low (V_{sat-}) pulse with duration of approximately $0.6\,RC$. It is useful for converting a square-wave input into a series of narrow output pulses. The input passes through a high-pass (AC coupling) filter consisting of components C and R. The resistor is connected to +12V rather than ground so that the op-amp's output will be at V_{sat+} whenever the input is unchanging. When the input transitions from V_{sat+} to V_{sat-} the falling edge will pass through the filter, momentarily reducing the voltage at the op-amp *+Input* to well below ground and causing the output to transition to V_{sat-}. Following the input transition the voltage at the *+Input* then relaxes back towards +12V with time constant RC. As the *+Input* voltage passes up through ground the op-amp output transitions back to V_{sat+}, completing the output pulse. The reverse-biased diode protects the op-amp *+Input* by shorting out rising edge input transitions which pass through the RC filter. Swapping the connections to the op-amp's + and − inputs will reverse the polarity of the circuit's output pulse. Interestingly, the circuit doesn't seem to work very well if you try to trigger on rising input edges by connecting R to the op-amp's −12V supply.

Op-amp comparators as logic gates

Although using op-amps as comparators to perform logic functions is not a practical approach for developing high-speed digital circuit applications, they can still be useful for simple logic calculations in your circuits. For example, consider the "logic gates" shown in Figure 4-15.

In each of these circuits a weighted mean of a set of input voltages is applied to one op-amp



AND/OR gate NAND/NOR gate

Figure 4-15: Simple logic gate applications of op-amp comparators. The generalized voltage divider applies a weighted mean which the op-amp compares to a reference voltage. When the sum exceeds the reference, the comparator output goes to V_{sat+} (left) or V_{sat-} (right).

input, which it compares to the reference voltage applied to its other input. The op-amp's output will be at either positive or negative saturation depending on the resulting sign of $v_+ - v_-$. These input voltages could be a variety of analog signals from various sources, or they might be outputs from other op-amp comparators thus inputting voltages of V_{sat+} or V_{sat-}.

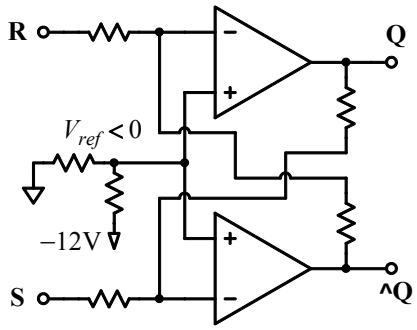
To see how this scheme might work, consider the left-hand circuit of Figure 4-15, where the set of inputs are applied to the op-amp's *+Input*. For simplicity's sake, we'll further assume that all the resistors are equal (10k, say), and that the input voltages come from saturated op-amp outputs. If we want to perform a logic AND of these inputs (all inputs must be at V_{sat+} for the circuit output to be at V_{sat+}), then the reference voltage V_{ref} should be set high enough that if just one input were at V_{sat-} then the mean of the inputs would be less than V_{ref}. For three inputs as shown, setting, say $V_{ref} > V_{sat+}/2$ should work. Similarly, for a logic OR function V_{ref} should be set such that only one input would be required to be at V_{sat+} to result in the mean exceeding V_{ref}.

More subtle requirements on the combination of input voltages required for the comparator output to be at V_{sat+} versus V_{sat-} could be implemented. For example, by properly selecting the value of V_{ref} you could require a simple majority of a set of, say, five input signals to be at V_{sat+} for the comparator output to change. You could also input a combination of various signals and reference voltages to voltage dividers attached to both op-amp inputs so that any arbitrary combination of high (V_{sat+}) and low (V_{sat-}) input values would be required to change the comparator's output. Of course, you can also configure the circuit as a Schmitt trigger to provide noise immunity and faster output transitions.

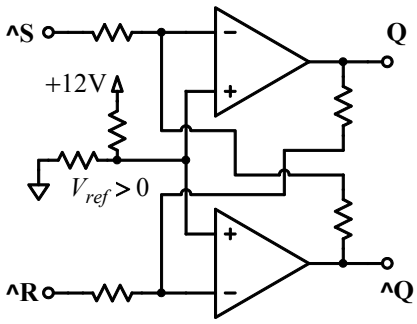
RS flip-flop implementations using op-amps

Figure 4-16 on page 4-23 shows two ways to implement an *RS* flip-flop using two op-amp comparators. As you can see, each op-amp's output is combined with an input signal and presented to the other op-amp's *−Input*. The resistors used to combine these voltages should be equal and preferably have values of at least 10k.

Consider first the upper circuit shown in Figure 4-16: its reference voltage V_{ref} should be set using a voltage divider to somewhat less than 0V: say about $V_{sat-}/2$. In this way, each op-amp's *−Input* voltage will be less than V_{ref} only when both voltages input to it are at V_{sat-} (*low*). This makes the upper circuit's **R** and **S** inputs *active high* (V_{sat+}). Bringing one of these inputs *high* will cause its op-amp output to go *low*. Now both voltages to the other op-amp's *−Input* are *low*, causing that op-amp's output to go *high*. This output will then sustain the flip-flop's state when the original input is returned to *low*. If both **R** and **S** inputs are *high* then both op-amp outputs will be *low* (the *undefined* flip-flop state). The last input to return *low* will then set the flip-flop state and restore normal operation.



S (set)	R (reset)	Q	^Q
Low	Low	unchanged	unchanged
High	Low	High	Low
Low	***High***	Low	High
High	***High***	Low	Low



^S	^R	Q	^Q
High	High	unchanged	unchanged
Low	High	High	Low
High	***Low***	Low	High
Low	***Low***	High	High

Figure 4-16: *RS* flip-flops using op-amps. The state tables use "High" for V_{sat+} and "Low" for V_{sat-}. The top circuit uses high values for S and R to select the flip-flop state, whereas the bottom circuit uses low values (^S and ^R). The only difference between the two circuits is the the reference voltage divider used for V_{ref}: V_{ref} < 0 for the top circuit vs. V_{ref} > 0 for the bottom. The resistors attached to the op-amp *–Inputs* should all be equal so that equal weights are given to the R and S inputs and the op-amps' Q and ^Q outputs. The resistors in the reference voltage dividers can also be equal, setting V_{ref} to half the corresponding supply voltage.

The lower circuit in Figure 4-16 differs only in the value chosen for its reference voltage V_{ref}. For this circuit it is chosen to be greater than 0, say $V_{sat+}/2$. Now each op-amp's *−Input* voltage will be greater than V_{ref} only when both voltages input to it are at V_{sat+} (*high*). Consequently, this version's inputs are *active low* (V_{sat-}), so they become **^S** and **^R** rather than **R** and **S**. Note also that the undefined state for this circuit version will drive both op-amp outputs *high*.

The 555 as RS flip-flop

The circuit at right shows how you can use the 555 IC as a simple *RS* flip-flop. Its *Trigger* and *Threshold* inputs can be used without bothering with any sort of external RC timing components. *Trigger* is an *inverted* **S** input (bring it below $1/3V_{supply}$ to set the **Q** output); *Threshold* is a *noninverted* **R** input (bring it above $2/3V_{supply}$ to reset the **Q** output). You still need to connect pins 1, 4, 5, and 8 as usual; the *Discharge* pin 7 can be left unconnected. Make sure you keep the input voltages between the 555 supply voltages (pins 1 and 8)!

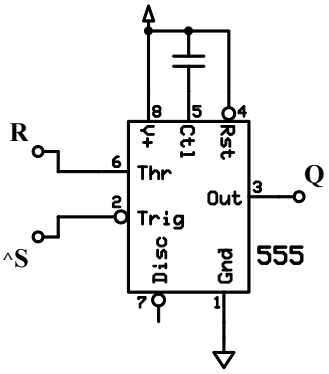


Figure 4-17: Using the 555's internal RS flip-flop.

Interfacing an op-amp output to the 555

If you are using +12V for the 555's supply voltage and your op-amps are powered using ±12V, then an effective way to couple an op-amp output to the 555 *Trigger* input is to use the circuit shown at right. The diode and resistor combination on the op-amp's output keeps the input to the 555 from going below ground: when the op-amp's output is negative, the diode turns off and the 555 input is connected to ground through the resistor (essentially a half-wave rectifier). The resistor's value should be at least 10k to keep the op-amp's output current reasonable. Make sure you orient the diode correctly!

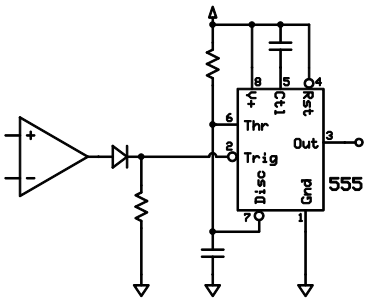


Figure 4-18: Interfacing an op-amp output to the 555's *Trigger* input.